

CLAIMS

1. A synchronous DRAM comprising:
one memory array divided into a plurality
of memory blocks;

mode storage units so disposed in a
plurality of stages as to correspond to said memory
blocks, for storing control information for defining
operation modes of said memory blocks;

a setting unit for setting the control
information designated by a mode setting instruction to
said mode storage unit corresponding to said memory block
designated by said mode setting instruction in accordance
with said mode setting instruction outputted from a
plurality of controllers;

a mode selection unit for selecting said
mode storage unit corresponding to said memory block
containing a memory cell designated by an address
inputted; and

an access unit for executing an access
operation in synchronism with a predetermined clock
signal for the corresponding one of said memory blocks in
accordance with the control information stored in said
mode storage unit selected.

2. A synchronous DRAM according to claim 1,
wherein said plurality of memory blocks is constituted by
continuous memory cells designated by addresses.

3. A synchronous DRAM according to claim 1,
wherein said plurality of memory blocks coincides with
memory banks.

4. A synchronous DRAM according to claim 1,
wherein said setting unit includes an object selection
unit for selecting said mode storage unit corresponding
to a bit train on the basis of said bit train in the data
outputted as a part of said mode setting instruction from
a plurality of controllers, and setting it as a setting
object of the control information.

5. A synchronous DRAM according to claim 4,

wherein said bit train is a bit train contained in the address outputted to an address bus.

6. A synchronous DRAM according to claim 5, wherein said bit train contained in said address is a bit train assigned to a test mode.

7. A synchronous DRAM according to claim 5, wherein said bit train contained in said address is a bit train assigned to a burst length.

8. A synchronous DRAM according to claim 5, wherein said bit train contained in said address is a bit train assigned to CAS latency.

9. A synchronous DRAM according to claim 4, wherein said bit train is a bit train contained in the data outputted to said data bus.

10. A synchronous DRAM according to claim 4, wherein said setting unit includes an input unit for inputting the control information to said mode storage unit as a setting object on the basis of the bit train outputted as a part of the mode setting instruction by said plurality of controllers to said address bus.

11. A synchronous DRAM according to claim 1, wherein said mode selection unit includes:

a selector for acquiring information designating said memory blocks and selecting the control data outputted from the corresponding one of said mode register sets; and

an address generation unit for generating a series of addresses in accordance with the operation mode inputted.

12. A synchronous DRAM according to claim 1, wherein said access unit includes:

an address decoder for decoding an address input and designating the memory cell; and

an input/output control circuit for executing an access processing corresponding to the operation mode designated, for the designated memory cell.